CASCADABLE DIGITAL FILTER PROCESSOR EMPLOYING MOVING COEFFICIENTS

BACKGROUND OF THE INVENTION

This invention relates generally to dedicated systolic processing arrays, and more particularly the invention relates to a pipelined digital filter processor employing moving coefficients.

The digital filter processor (DFP), also referred to as a finite impulse response (FIR) processor or convolver, forms vector operations in the form of

$$Y_n = \sum_{i=o}^{k-1} X_{n-i}\, C_i$$

where

X_{n-i}—input samples

Y_n—output filtered signal

c_i—filter coefficients

k—filter length, number of taps

A number of DFP integrated circuits are commercially available. Typically, sampled data is fed sequentially to multipliers having fixed coefficients, and the partial products are then summed and outputed.

SUMMARY OF THE INVENTION

An object of the present invention is a DFP having increased processing speed.

Another object of the invention is a DFP circuit which is flexible in application.

Still another object of the invention is a DFP circuit having a plurality of multiplier accumulators that are accessible through a common bus, and may operate in four modes according to the number representation (i.e. 2's complement, unsigned and mixed modes) of the multiplicands.

Another object of the invention is a DFP circuit which can be cascaded for operation on data with greater filter lengths.

Yet another of the invention is a DFP circuit that can perform sample rate reduction or decimation.

Another object of the invention is a DFP circuit that can be concatenated for longer word length of data and coefficients.

Briefly, a DFP circuit in accordance with the invention includes a plurality of cells organized to operate on data, that enters all the cells in parallel and includes a sign mode bit for 2's complement or unsigned representation, with filter coefficients being pipelined to the individual cells as the data is supplied in parallel to the cells. Each cell has a multiplier/accumulator (MAC), and each MAC is connected through a common multiplex bus (MUX) to a cell output/accumulator.

Filters of increased lengths can be created by cascading together several DFP circuits or by recycling in a single circuit. By using multiple circuits the sample rate need not be reduced. By recycling data in a one or more circuits the increased filter length is accommodated by reducing sample rate. The circuits can be operated in parallel to get maximum sample rate by computing partial products and then adding to obtain a final result.

Coefficients in each cell are connected to adjacent cells through a plurality of registers and multiplexers. The registers allow the coefficients to be delayed through the cell by one or more clocks for resampling or decimation for rate reduction. The decimation registers can be employed also to provide convolution of image points. The coefficients and data include a sign mode bit which specifies the 2's complement or unsigned number representation.

The invention and objects and features thereof will be more readily apparent from the following detailed description and appended claims when taken with the drawing.

BRIEF DESCRIPTION OF THE DRAWING

FIG. **1** is a logic symbol and signal identification for a DFP circuit in accordance with one embodiment of the invention.

FIG. **2** is a functional block diagram of the DFP of FIG. **1**.

FIG. **3** is a functional block diagram of one cell in the DFP circuit of FIG. **2**.

FIG. **4** is a functional block diagram of the output stage of the DFP circuit of FIG. **2**.

FIG. **5** is a table illustrating operation of the DFP circuit of FIG. **2** in a simple four tap filter mode of operation.

FIG. **6** is a schematic of the four tap filter operation using the logic symbol of FIG. **1**.

FIG. **7** is a timing diagram for the four tap filter operation.

FIG. **8** is a functional block diagram of an eight tap FIR implemented by cascading two DFP's of the specified embodiment illustrated in FIG. **1**.

FIG. **9** is a timing diagram of the eight tap FIR cascade operation of FIG. **8**.

FIG. **10** is a table illustrating operation of the single circuit for implementation of an eight tap filter.

FIG. **11** is a schematic diagram of circuitry with DFP word size extension.

FIG. **12** is a table illustrating operation of a single DFP circuit with word size extension.

FIG. **13** is a timing diagram of the operation illustrated in the table of FIG. **12**.

FIG. **14** is a table illustrating operation of the circuitry of FIG. **2** in a decimate by two mode of operation.

FIG. **15** is a timing diagram of the operation illustrated in the table of FIG. **14**.

FIG. **16** is a schematic diagram of the circuitry of FIG. **2** for image convolution.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

The invention has been reduced to practice in a digital filter processor device designated ZR33481 to be announced by Zoran Corporation, Assignee of the application. FIG. **1** is a logic symbol diagram and pin definition for the device. The device **10** comprises four multiplier/accumulator (MAC) stages cascaded internally and a shift and add output stage, all in a single integrated circuit. Each MAC stage contains an 8×8 bit multiplier. This multiplier may operate in 4 modes—according to the mode bit of the multiplicands: 2's complement$\times$unsigned, 2's complement$\times$2's complement, unsigned$\times$unsigned, unsigned$\times$two's complement, a 26 bit accumulator and three decimation registers. The output stage contains an additional 26 bit accumulator which can add the contents of any MAC stage accumulator to the output stage accumulator shifted right by 8 bits. This feature is used in implementing more than 8 bits MAC (data or coefficients) with several cells. As will be described below, the DFP can be configured to